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Fault tolerant systems have the capability of withstanding defects and are able to provide specified output despite faults occurring or having occurred. Similarly design for testability (DFT) is a technique that facilitates ease of testing of complicated electronic systems.

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Features A systematic study of the various fault tolerant architectures in use. An in depth review of the basic characteristics of self checking logic detailed descriptions of all the major hardware techniques that may be used in fault tolerant and testable design.

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Abstract: We propose a novel C-testable technique for the fast-Fourier-transform (FFT) networks. Only 18 test patterns are required to achieve 100% coverage of combinational single cell faults and interconnect stuck-at faults for the FFT network. A fault tolerant design for the FFT network also has been proposed.

Testability and test generation for majority voting fault ...
Based on this testable design, fault-tolerant approaches at the bit level and the multiply-subtract-add (MSA) module level are proposed, respectively.

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The testability conditions apply to both combinational and sequential logic circuits and result in testable majority voting based fault-tolerant circuits without additional testability circuitry. Alternatively, the testability conditions facilitate the application of structured design for testability and Built-In Self-Test techniques to fault-tolerant circuits in a systematic manner.

Easily testable and fault-tolerant FFT butterfly networks ...
Parag Lala: "Fault tolerant and Fault Testable Digital Design"; (Prentice Hall International). It is not available from the publisher. The instructor has a few copies of this text which may be borrowed. Israel Koren & C. Mani Krishna: "Fault-Tolerant Systems" (Morgan Kaufmann)

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Fault tolerant and fault testable hardware design . 1985. Abstract. No abstract available. Cited By. Angiolini F, Jamaa M, Atienza D, Benini L and De Micheli G Interactive presentation: Improving the fault tolerance of nanometric PLA designs Proceedings of the conference on Design, automation and test in Europe, (570-575)

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The basics for these advances lies in the ability to design microelectronics based systems which are much more fault tolerant and more easily testable than those which have been developed to date. The current activities in the design of testable/fault tolerant integrated circuits are reviewed and areas for future emphasis are suggested.

The use of fault tolerant and testable high performance ...
In this paper, we first propose a C-testable FFT network design. Only 20 test patterns are required to cover all combinational single-cell faults and interconnect stuck-at and break faults for the FFT network, regardless of its size. A spare-row based fault-tolerant FFT network design is subsequently proposed.

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